61 THE CHIPS TO SYSTEMS CONFERENCE

SHAPING THE NEXT GENERATION OF ELECTRONICS

JUNE 23-27, 2024

MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA

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Automated Topology based Pin Access Checker for Correct by Construction Standard Cells Design

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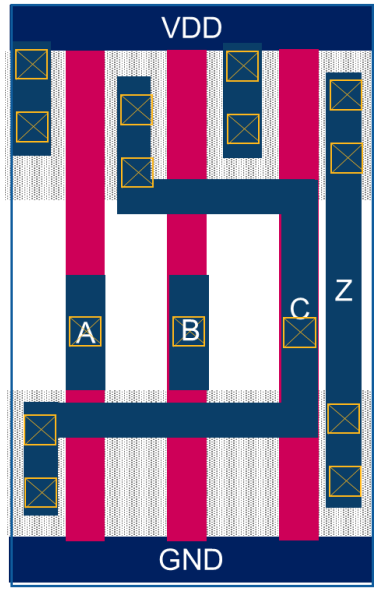
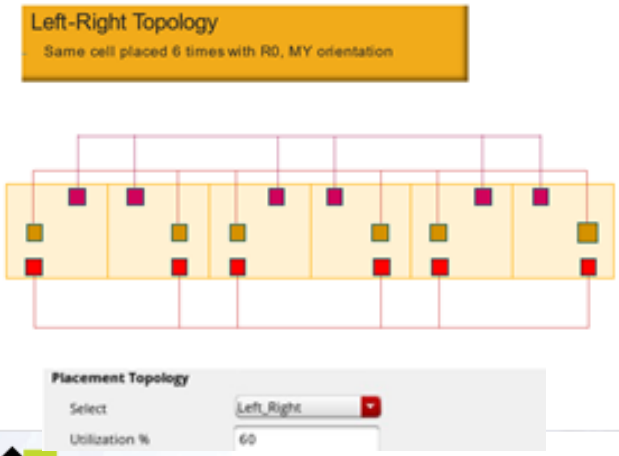
Motivation

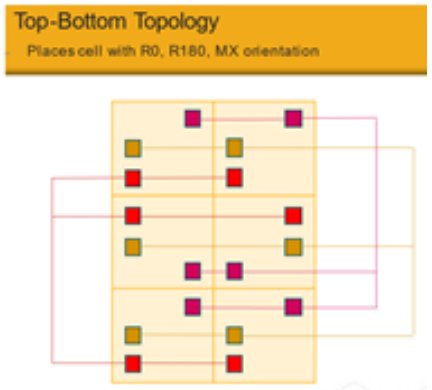
- Pin accessibility is crucial to ensure routability at SoC implementation
  - Due to pin accessibility issues caught late in SoC implementation cycle, tape out can be delayed impacting time to market
- To capture pin accessibility issues beforehand, standard cells can be placed and routed in SoC like conditions
- Atleast 200-500 cells in each standard cells library
  - Not possible to validate each cell's pin accessibility manually
  - Cells in SoC come from various standard cells libraries, need to validate them with respect to each other
- Standard Cells could be surrounded by a set of cells which could mimic SoC like placement

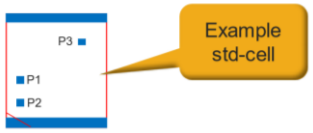
A Typical Std Cell

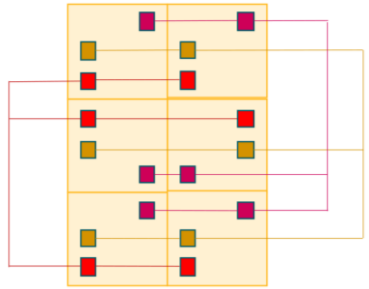
Input Pins : A, B, C
Output Pin : Z
Supply : VDD
Ground : GND





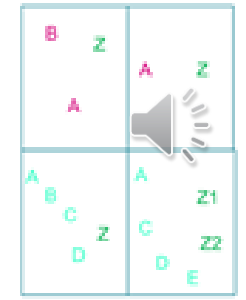






Single Cell Topology
Same Instance pins connected with each other

Multi Cell Topology
Novel Connectivity Computation based on number of input and output pins



Flow Overview

Design Tech Data + Technology Lef = Technology Library for router

Design Inputs
Technology lef file, Library/Cells, Placement topology

Routing Options
Max routing layer, via type, critical net

Virtuoso Studio Layout
Placement according to user specified topology

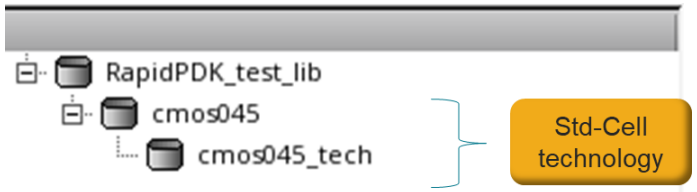
Innovus
Routing of Placed topology

Output
DRC Report
Via Statistics
Placed and Routed layout view

- **Technology LEF**: Select input technology LEF file which contains routing data.
- **Design Information**: Select Library, std-cells and layout/abstract views on which tool will run
- **Output Directory**: Name of Directory for storing resultant views and auxiliary files

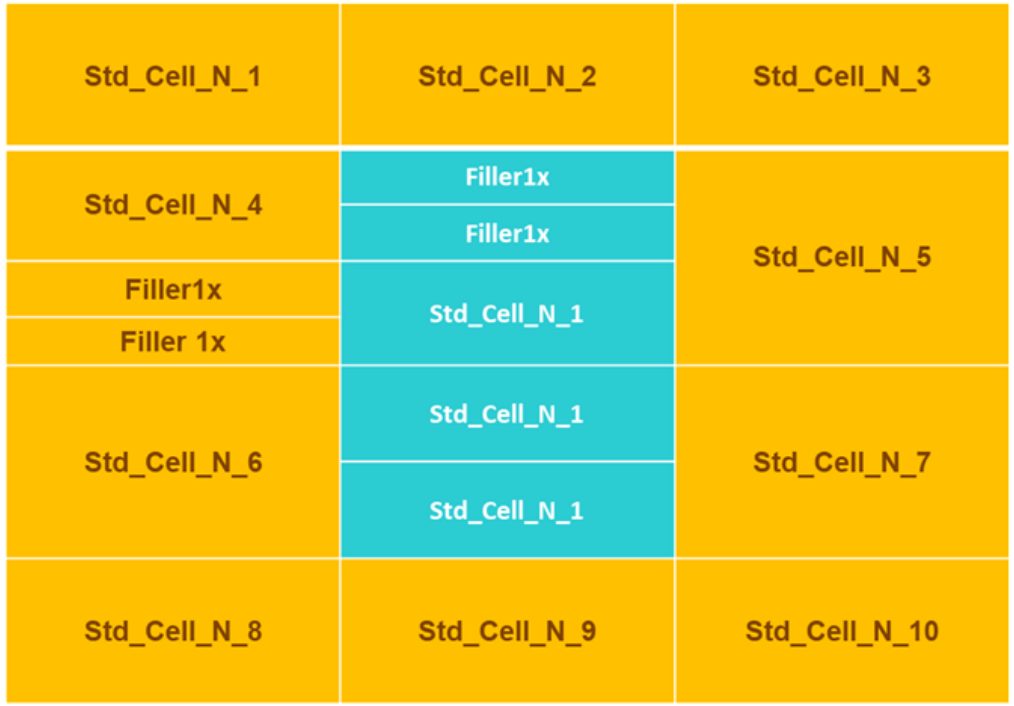
Integration with Innovus

- Rapid PDK is created dynamically by PAC from technology LEF and technology attached with Standard Cell Library.

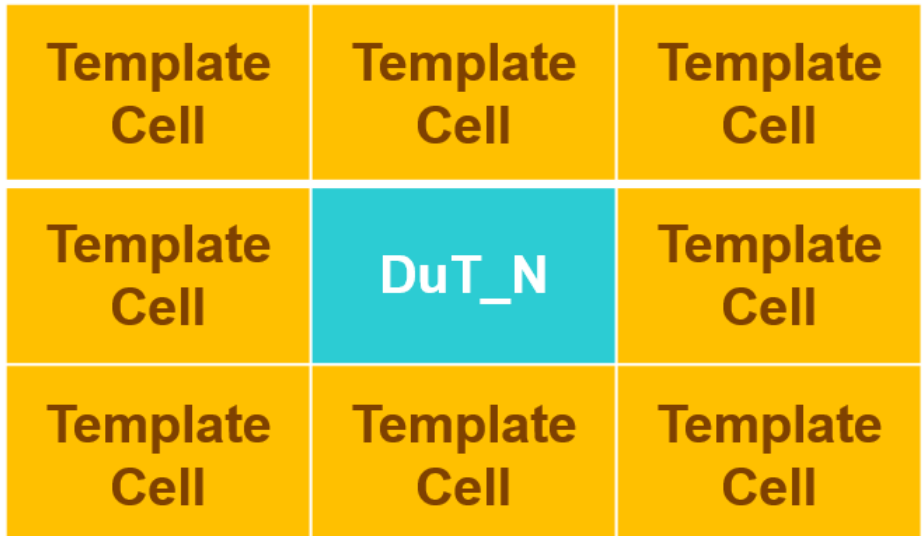


Template Topology

- Typical standard cells could consist varying width, fillers are required to ensure placement topology has continuous rail and no empty spaces are left
- The number of filler cells and repetition of DuT (vertically or horizontally) is automatically calculated by tool to mimic SoC like placement
- The flow is iterated over the complete library where each cell is replaced for DuT



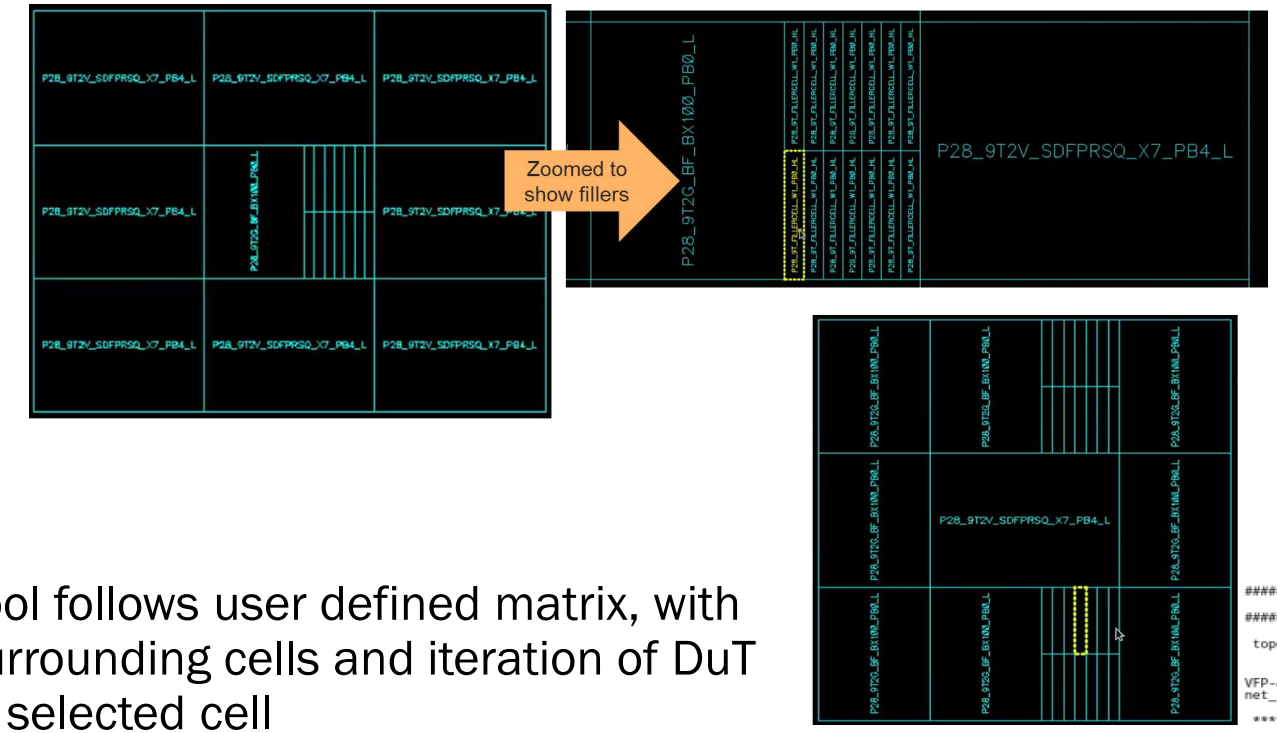
Custom Topology with Surrounding Cells and Fillers

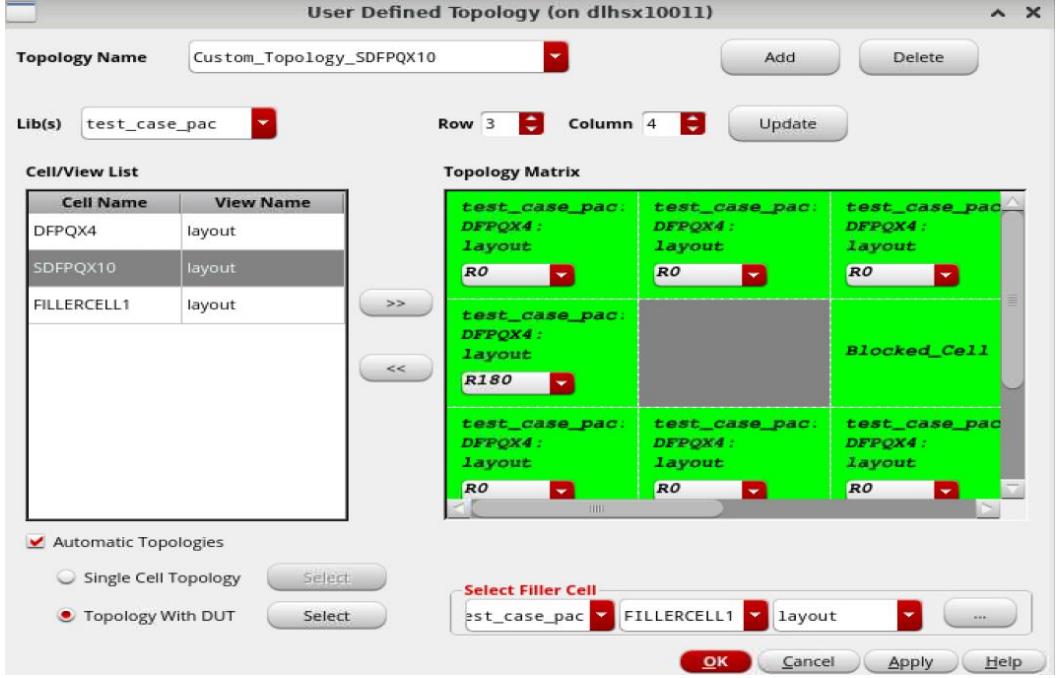


Single Cell Topology with Surrounding Cell iterating DuT

Single Cell Topology with iterating DuT

Results

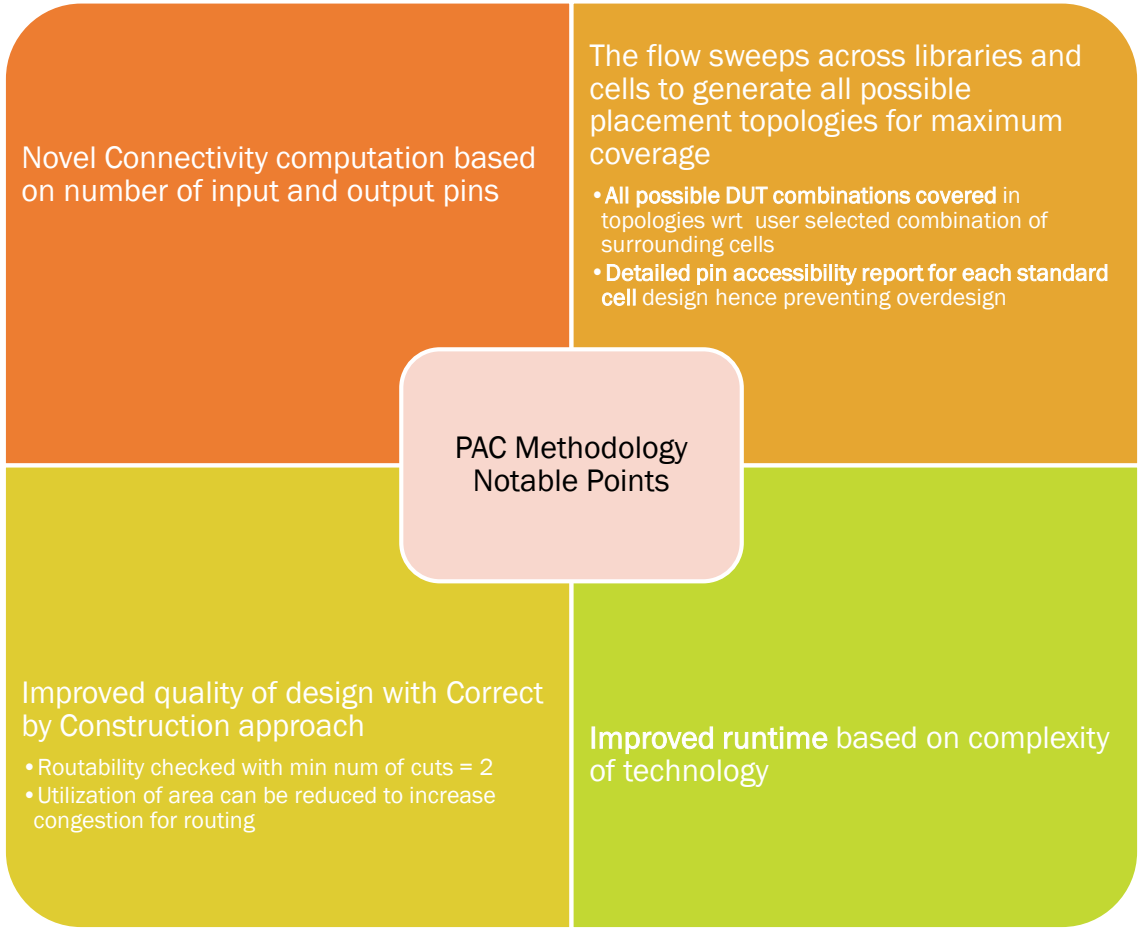




- Tool follows user defined matrix, with surrounding cells and iteration of DuT in selected cell
- In cases when DUT and surrounding cell is of different height, generated topology is automatically adjusted (cells added/deleted) to cater supply rails uniform
- To ensure that placement is uniform and rails are continuous, filler cells (FILLERCELL1) are inserted as and where required

```
##################################################################################################################################
                                                Pin Accessibility Checker Report
##################################################################################################################################
 topologiesViews:Custom_Topology_SDFPQX10:layout_60_M3          Total Violations: 0 Violations        topologiesViews:Custom_Topology_SDFPQX10:layout

VFP-40032: Pin Accessibilty Checker will consider net(s) 'gnd, vdd, net_inst_16_P__12, net_inst_15_P__12, net_inst_12_P__12, net_inst_11_P__12, net_
net_inst_6_P__12, net_inst_5_P__12, net_inst_4_P__12, net_inst_1_P__12, net_inst_0_P__12' as critical nets.

******************** Critical Nets Via Statistics for cell Custom_Topology_SDFPQX10:layout_60_M3_routed ********************
    Net net_inst_10_P__12 : [inst_8 : D,CP]
    Layers              Single-Cuts              Double-Cuts
    #-----------------------------------------------------
    M1-M2               0                        1
    M2-M3               0                        3
    #-----------------------------------------------------

    Net net_inst_8_P__21 : [inst_8 : Q]
    Layers              Single-Cuts              Double-Cuts
    #-----------------------------------------------------
    M1-M2               0                        3
    M2-M3               0                        4
    #-----------------------------------------------------

    Net net_inst_7_P__21 : [inst_8 : TI,TE] [inst_7 : Q]
    Layers              Single-Cuts              Double-Cuts
    #-----------------------------------------------------
    M1-M2               0                        1
    M2-M3               1                        2
    #-----------------------------------------------------

    Net net_inst_6_P__12 : [inst_7 : D,CP]
    Layers              Single-Cuts              Double-Cuts
    #-----------------------------------------------------
    M1-M2               0                        1
    M2-M3               0                        3
    #-----------------------------------------------------

    Net net_inst_5_P__12 : [inst_7 : TI,TE]
    Layers              Single-Cuts              Double-Cuts
    #-----------------------------------------------------
    M1-M2               0                        1
    M2-M3               0                        4
    #-----------------------------------------------------

********************** Length of Metals in non-preferred direction for cell Custom_Topology_SDFPQX10:layout_60_M3_routed **********************
    Layer: M1 Preferred direction: vertical, Non Preferred direction: horizontal  Non preferred wire length: 0.83
    Layer: M2 Preferred direction: horizontal, Non Preferred direction: vertical  Non preferred wire length: 2.4
    Layer: M3 Preferred direction: vertical, Non Preferred direction: horizontal  Non preferred wire length: 10.494
```

Summary



Gains over Conventional Methodology

Category	Conventional	Proposed
Combinations	all possible combinations might be missed	user can change the set of environment cells for a DUTs depending upon the congestion
Analysis Stage	cells are analyzed at the end of library development flow	can be run on a set of cells even during library development stage
Topologies	No topologies created	DUT with itself topology User selected cells with DUT topology
Power Rail	Power rail width modification not possible	Power rail width can be modified as per customer request, to mimic SOC behavior for routing
Runtime	Overnight run for all technologies	For less complex technologies, the iterations completes by approx. 5 hours